IP Cores Design from Specifications to Production: Modeling, Verification, Optimization, and Protection (Analog Circuits and Signal Processing)

Khaled Salah Mohamed

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This book describes the life cycle process of IP cores, from specification to production, including IP modeling, verification, optimization, and protection. Various trade-offs in the design process are discussed, including those associated with many of the most common memory cores, controller IPs and system-on-chip (SoC) buses. Readers will also benefit from the author's practical coverage of new verification methodologies. such as bug localization, UVM, and scan-chain. A SoC case study is presented to compare traditional verification with the new verification methodologies.

Discusses the entire life cycle process of IP cores, from specification to production, including IP modeling, verification, optimization, and protection;

Introduce a deep introduction for Verilog for both implementation and verification point of view.

Demonstrates how to use IP in applications such as memory controllers and SoC buses.

Describes a new verification methodology called bug localization;

Presents a novel scan-chain methodology for RTL debugging;

Enables readers to employ UVM methodology in straightforward, practical terms.

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